UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/054,847	01/25/2002	Howard E. Rhodes	M4065.0295/P295-A	9091

24998 7590 06/19/2003

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	4

DATE MAILED: 06/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/054,847	RHODES, HOWARD E.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *90-116* is/are pending in the application.

4a) Of the above claim(s) *106-111* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *90-105 and 112-116* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/054,847, which is a divisional of Application Serial No. 09/650,432, filed on 28 August 2000. Currently, claims 90-116 are pending.

Election/Restrictions

2. This application contains claims directed to the following patentably distinct species of the claimed invention: I. the species disclosed in figs. 1-12 (claims 90-105 and 112-116), and II. the species disclosed in figs. 13 and 14 (claims 106-111).

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claim is generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If

claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

3. During a telephone conversation with Thomas J. D'Amico on 30 May 203 a provisional election was made without traverse to prosecute the invention of Group I, claims 90-105 and 112-116. Affirmation of this election must be made by applicant in replying to this Office action. Claims 106-111 have been withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Information Disclosure Statement

The parent application was in the process of being issued at the time of examination of the current application, and was therefore unavailable. For this reason, the non-patent literature references, which were cited in the information disclosure statement filed on 25 January 2002, have not been considered. However, once the application becomes available, the examiner will consider the non-patent literature references. In response to this action, please submit a copy of the PTO-1449 filed on 25

January 2003. The examiner will attach an initialed and signed copy of the 1449 to the next action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. *Claims 90, 92, 96-103, 112, 115, and 116 are rejected under 35 U.S.C. 102(b) as being anticipated by Anderson et al. (US 5,112,762 B1).*

Anderson et al. disclose a method of forming a capacitor (figs. 2, 3, 4, 4a-4d and accompanying text). The method comprises the steps of: providing a semiconductor substrate 48 having a doped layer 40 of a first conductivity type (fig. 4); forming a plurality of trenches 16a, 16b in the doped layer, each of said plurality of trenches having a plurality of sidewalls and a bottom (figs. 4b, 4c); doping the sides and bottom of each of the plurality of trenches to form a doped region 50 of a second conductivity type (fig. 4d); and forming an insulating layer 52 on the sides and bottom of each of said plurality of trenches over the doped region (fig. 3).

The method further comprises forming a conductive layer 32 on substantially all of an upper surface of the insulating layer (fig. 3).

The insulating layer 52 is a layer of silicon dioxide (col. 3, lines 19-22).

The first conductivity type is p-type, and the second conductivity type is n-type.

The semiconductor substrate is a silicon substrate (col. 3, lines 11-13).

The step of forming a plurality of trenches comprises a reactive ion etching process (col. 3, line 64-col. 4, line 4).

The step of forming a plurality of trenches comprises forming two trenches 16a, 16b (fig. 4c).

The doping step comprises ion implantation (col. 4, lines 17-21).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. *Claims 94 and 95 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson et al. in view of Wolf et al. (Silicon Processing for the VLSI Era – Vol. 1: Process Technology).*

As discussed above, Anderson et al. disclose forming a conductive layer 32 on substantially all of an upper surface of the insulating layer. The conductive layer is a polysilicon layer (col. 3, lines 19-22). Anderson et al. do not teach that the polysilicon

layer 32 is formed using chemical vapor deposition (CVD), or that the conductive layer is formed using a sputtering method.

Wolf et al. teach both the use of CVD (pages 177-178) and sputtering to form silicon films (page 335, first paragraph). Although sputtering may be used to deposit polysilicon, low pressure CVD (LPCVD) is the preferred deposition method.

It would have been obvious to one having ordinary skill in the art, at the time the invention was made, to form the polysilicon conductive layer 32 using LPCVD because a polysilicon layer deposited using LPCVD has excellent uniformity (page 177, third paragraph). It would have been obvious to one having ordinary skill in the art, at the time the invention was made, to form the polysilicon conductive layer 32 using a sputtering method because film thickness control is easily achieved, and step coverage and grain structure can be controlled (page 335, second paragraph).

6. *Claims 90-105 and 112-116 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes (US 6,232,626 B1).*

Rhodes discloses a method of forming a photosensor (figs. 5-11 and accompanying text). The method comprises the steps of: providing a semiconductor substrate 16 having a doped layer 20 of a first conductivity type (fig. 6); forming a trench 104 in the doped layer, the trench having a plurality of sidewalls and a bottom (fig. 7); doping the sides and bottom of the trench to form a doped region 26 of a second

conductivity type (fig. 9); and forming an insulating layer 100 on the sides and bottom of the trench over the doped region (fig. 10).

The photosensor can be a photodiode sensor (col. 8, lines 50-54).

The method further comprises a step of forming a conductive layer 102 on substantially all of an upper surface of the insulating layer (fig. 11).

The photosensor can be a photogate sensor (col. 8, lines 50-54).

Forming the conductive layer comprises a chemical vapor deposition step (col. 8, line 63-col. 9, line 1).

Forming the conductive layer comprises a sputtering step (col. 8, line 63-col. 9, line 1).

The insulating layer is a layer of silicon dioxide (col. 8, lines 44-50).

The first conductivity type is p-type, and the second conductivity type is n-type (col. 6, line 67-col. 7, line 3 and col. 7, lines 3-6).

The semiconductor substrate can be a silicon substrate (col. 6, lines46-56).

Forming the trench comprises a reactive ion etching process (col. 7, lines 49-58).

The doping step comprises ion implantation (col. 8, lines 12-26).

The doping step comprises multiple angled ion implantation (col. 8, lines 12-26).

The multiple angled ion implantation comprises four orthogonal angled implants at a dose of 1×10^{12} to $1 \times 10^{"}$ ions/cm^2, wherein a resist is placed on top of the substrate while implanting, and wherein the angle of implantation for each angled implant is

greater than 0, where tan $\theta_c = [(t+d)/(w)]$, where t is the thickness of the resist, d is the depth of the trench, and w is the width of the trench (col. 8, lines 12-26).

The dose of each implant can be $1x10^{13}$ to $1x10^{15}$ ions/cm^2 (col. 8, lines 12-26).

The dose of each implant can be $5x\ 10^{13}$ ions/cm^2 (col. 8, lines 12-26).

Rhodes lacks anticipation only in not forming a plurality of trenches in the doped layer 20. However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form a plurality of trenches in the doped layer, since the court has held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced (*In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (703) 305-7646. The examiner can normally be reached on Monday through Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JMJ
June 16, 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800